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10/666,709	09/19/2003	Hiroki Kanai	16869K-095200US	1998

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/666,709	KANAI ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7,12,13 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,12,13 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 January 2007 has been entered.

Status of Claims

2. Claims 5-7, 12, 13 and 17-19 are pending in the Application.

Claims 1-4, 8-11, 14-16 and 20-22 are cancelled.

Claims 5-7, 12, 13 and 17-19 are amended.

Claims 5-7, 12, 13 and 17-19 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 22 January 2007 in response to the office action mailed on 7 September 2006 have been fully considered, but are moot in view of the new ground(s) of rejection. It is worthy to note that it appears that Applicant failed to address the claim objections set forth in the previous Office correspondence. Those objections are therefore maintained, and restated below.

Claim Objections

4. Claims 13, 17, and 19 are objected to because of the following informalities:

As for claims 13 and 19, the phrase "the address" as recited in line 16 of claim 13 (line 14 of claim 19) should be changed to "an address".

As for claim 17, the phrase "the information processor" as recited in lines 3-4 of this claim should be changed to "an information processor".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5-7,12, and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the local cache memory" in 13 of the claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, each controller contains "a local cache memory", which is being claimed here?

A similar rejection applies to claim 6 for the phrase "the first cache memory" in line 14; claim 7 for the phrase "the first cache memory" in line 21; claim 12 for the phrase "the second cache memory" in line 28; claim 17 for the phrase "the local cache memory" in line 15; claim 18 for the phrase "the second cache memory" in line 11; claim

18 for the phrase "the first cache memory" in line 17; and claim 19 for the phrase "the first cache memory" in lines 20-21.

As for claim 12, the phrase "the second cache memories" and in line 9 lacks antecedent basis, as "second cache memories" are not previously set forth within the claim. Additionally, "the information processor" as recited in lines 12-13 lacks antecedent basis, as "an information processor" is not previously set forth within the claim. Lastly, "the temporarily stored data" as recited in line 15 lacks antecedent basis as no data has been previously stored. Note the first cache memory recited in line 12 is *for* storing data, however the claim fails to recite the data actually being stored within that particular cache.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-6, 12 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Dewey et al. (US Patent 5,724,501), hereinafter Dewey, in further view of Mathiske et al. (US PG Publication 2002/0107667 A1), hereinafter Mathiske.

As for claims 5 and 17, Dewey teaches a method (as per claim 5, and medium per claim 17) for writing data to a cache memory wherein a data write-in request is issued from an information processor to a storage control apparatus, the storage control

apparatus including a plurality of the channel control units (Fig. 7, elements 401 and 401') each having an interface with the information processor; a disk control unit (Fig. 7, element 414) having an interface with a storage device (Fig. 7, element 404) for storing data; a local cache memory (Fig. 7, elements 422 and 422') disposed in each channel control unit for temporarily storing data to be interchanged between the information processor and the storage device; a dedicated data transfer path between at least two of the local cache memories ((Fig. 7, element 426); a connector unit to provide data paths among the plurality of channel control units and the disk control unit separate from the dedicated data transfer path (Fig. 7, the path connecting disk interfaces (414, 412, etc.) and (414', 412', etc.) not labeled in the figure), comprising:

receiving data to be written from the information processor (Fig. 7, element 401 – the control unit contains logic to receive data transmitted from the host (not explicitly shown in Fig. 7));

writing the data to be written to the local cache memory of the first channel control unit (both the hosts and the control units are capable of writing data to the cache);

transmitting the data to be written through the dedicated data transfer path to a second channel control unit connected to the first channel control unit (the control unit is capable of transmitting data to the other control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8);

writing the transmitted data to the local memory of the second channel control unit (data is transferred between each of the local cache memories through the dump link (col. 2, line 54 through col. 3, line 8);

receiving through the dedicated data transfer path an acknowledgement indicating that writing of the transmitted data to the local cache memory disposed in the second channel control unit has completed (both the hosts and the control units are capable of receiving acknowledgements sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7); and

transmitting the acknowledgement to the information processor to notify the information processor that data written to the local cache memory of the second channel control unit has completed (both the hosts and the control units are capable of receiving acknowledgements via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7).

Though Dewey teaches memories (i.e. hard drives) as being connected through the connector unit (Fig. 7, elements 404, 406 and 408), he fails to teach a global cache memory. He further fails to teach wherein if the local cache memory does not have sufficient capacity to store the data to be written then first transmitting an amount of data stored in the local cache memory to the global cache memory by way of the connector unit in order to obtain sufficient capacity in the local cache memory to store the data to be written as recited in these claims.

Mathiske however teaches an apparatus which uses a global store buffer in conjunction with local store buffers. The global buffer is available to the system to handle overflows of the local buffers. More specifically, once it is determined that the local buffer does not contain sufficient capacity to store the data to be written to the buffer, the local buffer is flushed to the global buffer to obtain additional capacity (see paragraphs 0053 through 0056, all lines and Fig. 2, elements 200 and 210).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Dewey to further include Mathiske's bag-to-set buffering system. By doing so, Dewey would have a means of preventing data loss by mitigating the dangers of data buffer overflow in his RAM devices by writing the data to a backup memory (i.e. global) before such an overflow occurs, rather being restricted to preventing data loss only in the case of a controller failure as presently taught by Dewey in col. 11, line 66 through col. 12, line 12.

As for claims 6, 12 and 18, Dewey teaches a method (as in claim 6, control unit as in claim 12, and medium as in claim 18) in a storage control apparatus for reading in

data stored in a second cache memory to a first cache, the storage control apparatus including a plurality of channel control units each having an interface with an information processor; a disk control unit having an interface with a storage device for storing data; a plurality of first cache memories each being disposed in one of the channel control units for storing temporarily data to be interchanged between the information processor and the storage device, the first cache memory of at least two of the channel control units connected to one another through a dedicated data transfer path; and a connector unit to provide data paths among the plurality of channel control units, and the disk control unit separate from the dedicated data transfer path, the connector unit connected to a second memory, (see the rejection of claim 1 for the mapping of these elements), comprising:

a first cache memory for temporarily storing data to be interchanged between the information processor and the storage device, the first cache memory of at least two of the channel control units being connected to one another by the dedicated data transfer path for storing mutually the temporarily stored data (as discussed in claim 5, *supra*);

transmitting (via a transmitter/interface) a read-out command for data stored in the second cache memory, acquiring the data from the second cache memory, writing the acquired data to the first cache memory of the first channel control unit (col. 2, line 54 through col. 3, line 8 – Dewey's system works by sending a request from one control unit to another. The request allows data to be copied from one control unit's cache to the other control unit's cache for data

redundancy. By this means, one control unit can access data contained within the cache of the other control unit, and store said data in order to maintain data consistency within the caches);

Dewey further teaches transmitting the acquired data through the dedicated data transfer path from the first cache memory of the first channel control unit to the first cache memory of a second channel control unit connected to the first channel control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches receiving an acknowledgements from the second channel control unit indicating that the acquired data has been written to the first cache memory of the second channel control unit (Col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7).

Though Dewey teaches memories (i.e. hard drives) as being connected through the connector unit (Fig. 7, elements 404, 406 and 408), he fails to teach a global (second) cache memory. He further fails to teach wherein if the local (first) cache memory does not have sufficient capacity to store the data to be written then first transmitting an amount of data stored in the local cache memory to the global cache memory by way of the connector unit in order to obtain sufficient capacity in the local cache memory to store the data to be written as recited in these claims.

Mathiske however teaches an apparatus which uses a global store buffer in conjunction with local store buffers. The global buffer is available to the system to handle overflows of the local buffers. More specifically, once it is determined that the local buffer does not contain sufficient capacity to store the data to be written to the buffer, the local buffer is flushed to the global buffer to obtain additional capacity (see paragraphs 0053 through 0056, all lines and Fig. 2, elements 200 and 210).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Dewey to further include Mathiske's bag-to-set buffering system. By doing so, Dewey would have a means of preventing data loss by mitigating the dangers of data buffer overflow in his RAM devices by writing the data to a backup memory (i.e. global) before such an overflow occurs, rather being restricted to preventing data loss only in the case of a controller failure as presently taught by Dewey in col. 11, line 66 through col. 12, line 12.

7. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya et al. (US PG Publication 2001/0056527 A1), hereinafter Ninomiya, in further view of Dewey (US Patent 5,724,501), and in further view of Mathiske (US PG Publication 2002/0107667 A1).

As for claims 5 and 17, Ninomiya teaches a method (as per claim 5, and medium per claim 17) for writing data to a cache memory wherein a data write-in request is issued from an information processor to a storage control apparatus, the storage control apparatus including a plurality of the channel control units (Fig. 1, element 1) each having an interface with the information processor; a disk control unit

(Fig. 1, element 2) having an interface with a storage device (Fig. 1, the disks (elements 5) interface with the disk adapters) for storing data; a local cache memory (Fig. 1, element 3) disposed in each channel control unit for temporarily storing data to be interchanged between the information processor and the storage device; a dedicated data transfer path between at least two of the local cache memories ((Fig. 1, element 5); a connector unit to provide data paths among the plurality of channel control units and the disk control unit separate from the dedicated data transfer path (Fig. 1, element 4 depicts a redundant path, therefore communication via the channel and disk control units can occur on separate paths), comprising:

receiving data to be written from the information processor (Fig. 2, element 1 – the host adaptor contains logic to receive data transmitted from the processor – paragraph 0041, all lines. Also, though not shown in Fig. 1 explicitly, each host adaptor is connected to a processor – paragraph 0036, all lines);

writing the data to be written to the local cache memory of a first channel control unit (both the disk adaptor and host adaptor are capable of writing data to the cache – see paragraphs 0037 and 0038, all lines);

transmitting to the information processor the acknowledgement to the information processor to notify the information processor that data written to the cache memory of the second channel control unit has completed (paragraph 0037, the host adaptor contains the logic (referring again to Fig. 2, element 1) which is used to transmit the report to the host device that writing to the cache is complete).

writing the transmitted data to the local memory of the second channel control unit (paragraph 0037, the host adaptor contains the logic (referring again to Fig. 2, element 1) which is used to transmit the report to the host device that writing to the cache is complete);

Ninomiya fails to teach transmitting to the other control unit and receiving the acknowledgment from the other control unit.

Dewey however teaches receiving through the dedicated data transfer path an acknowledgement indicating that writing of the transmitted data to the cache memory disposed in the second channel control unit has completed (both the hosts and the control units are capable of receiving acknowledgements sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7); and transmitting the acknowledgement to the information processor to notify the information processor that data written to the cache memory of the second channel control unit has completed (both the hosts and the control units are capable of receiving acknowledgements via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to

recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7).

Additionally, Ninomiya fails to teach a global (second) cache memory, and further fails to teach wherein if the local (first) cache memory does not have sufficient capacity to store the data to be written then first transmitting an amount of data stored in the local cache memory to the global cache memory by way of the connector unit in order to obtain sufficient capacity in the local cache memory to store the data to be written as recited in these claims.

Mathiske however teaches an apparatus which uses a global store buffer in conjunction with local store buffers. The global buffer is available to the system to handle overflows of the local buffers. More specifically, once it is determined that the local buffer does not contain sufficient capacity to store the data to be written to the buffer, the local buffer is flushed to the global buffer to obtain additional capacity (see paragraphs 0053 through 0056, all lines and Fig. 2, elements 200 and 210).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Ninomiya to further include Dewey's quick recovery system of write cache. By doing so, Ninomiya would benefit by having a system that is not only capable of mirroring data within his multiple control units for data recovery, but additionally one that exploits the benefits of an onboard mirroring technique, in which the hosts incur no additional latency due to the mirroring of data. This in effect can help optimize performance during normal host operation, and allow for the secondary links to be

constructed with limited bandwidth, since the coping only occurs on failures as taught by Dewey (col. 2, lines 8-20).

It would have further been obvious to one of ordinary skill in the art at the time of the invention for Ninomiya to further include Mathiske's bag-to-set buffering system. By doing so, Ninomiya would have a means of preventing data loss by mitigating the dangers of data buffer overflow in his RAM devices by writing the data to a backup memory (i.e. global) before such an overflow occurs, in a must faster fashion, rather being restricted to writing the data to slower the DASD devices disclosed by Ninomiya in Fig. 1, element 5.

8. Claims 7, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dewey (US Patent 5,724,501) , in view of Mathiske (US PG Publication 2002/0107667 A1), and in further view of La Fetra et al. (US Patent 5,155,828), hereinafter La Fetra.

As for claims 7, 13 and 19, Dewey teaches a method (as in claim 7, control unit as in claim 13, and medium as in claim 19) performed by a channel control unit for reading out data by a channel control unit for the case where a data read-out request is issued from an information processor to a storage control apparatus, the storage control apparatus including a plurality of the channel control units each having an interface with the information processor; a disk control unit having an interface with a storage device for storing data; a first cache memory in each of the channel control units for temporarily storing data to be interchanged between the information processor and the storage device, the first cache memory of at least two of the channel control units being

connected to one another through a dedicated data transfer path; a plurality of second cache memories; and a connector unit to provide data paths among the plurality of channel control units, and the disk control unit separate from the dedicated data transfer path, the connector unit connected to the second memories (see the rejection of claim 1 for the mapping of these elements), comprising:

receiving from the information processor a read-out command for data for which an address is specified (the processor is capable of accessing data from the cache via the metadata which includes the disk and cache address for data stored in the disk or caches respectively – col. 4, lines 16-27);

determining whether the data at the specified address is stored in the first cache memory of a first channel control unit (a cache hit or miss can be determined –col. 7, lines 13-38. Again the determination can be made using the metadata, which directs the host to the appropriate address of the cache);

acquiring the data from said one of the second memories, and writing the acquired data to the first cache memory of the first channel control unit (col. 2, line 54 through col. 3, line 8 – Dewey's system works by sending a request from one control unit to another. The request allows data to be copied from one control unit's cache to the other control unit's cache for data redundancy. By this means, one control unit can access data contained within the cache of the other control unit, and store said data in order to maintain data consistency within the caches. Additionally, once a read request is encountered, data will be acquired from both cache memories – col. 7, lines 31-61);

Dewey further teaches transmitting the acquired data through the dedicated data transfer path to a second channel control unit connected to the first channel control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches receiving from the second channel control unit an acknowledgement indicating that the writing of the acquired data to the first cache memory disposed in the control unit has completed - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7.

Dewey additionally teaches transmitting the acquired data to the information processor (the control unit is capable of transmitting data to the host via the host interface (Fig. 7, element 400)).

Dewey fails to teach transmitting the read-out command for the data to the one of the second cache memories if the data at the specified address is not stored in the first cache memory of the first channel control unit (rather he teaches acquiring the data from the disks – col. 7, lines 62-66).

La Fetra however teaches a computing system with a cache memory and an additional look-aside cache memory wherein a processor attempts to access a second cache memory, and in case of a miss, accesses a first cache memory before accessing the main memory col. 2, lines 11-36). It is worthy to note that since the L2 (i.e. first

cache) cache contains all of the data of L1 (i.e. second cache), Dewey would be able to maintain mirroring of the first cache by storing the same data in a section of the L2 cache in the second control unit (plus the additional data not stored in the L1 cache). This way if a miss occurs to L1, the processor can search L2 cache prior to accessing the disk.

Additionally, though Dewey teaches memories (i.e. hard drives) as being connected through the connector unit (Fig. 7, elements 404, 406 and 408), he fails to these units as global (second) cache memories. He further fails to teach wherein if the local (first) cache memory does not have sufficient capacity to store the data to be written then first transmitting an amount of data stored in the local cache memory to the global cache memory by way of the connector unit in order to obtain sufficient capacity in the local cache memory to store the data to be written as recited in these claims.

Mathiske however teaches an apparatus which uses a global store buffer in conjunction with local store buffers. The global buffer is available to the system to handle overflows of the local buffers. More specifically, once it is determined that the local buffer does not contain sufficient capacity to store the data to be written to the buffer, the local buffer is flushed to the global buffer to obtain additional capacity (see paragraphs 0053 through 0056, all lines and Fig. 2, elements 200 and 210).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Dewey to further include La Fetra's system with a cache memory and look-aside cache memory into his own system of mirroring data. By doing so, Dewey would have an extra level of hierarchy in his cache system in order to retrieve requested data

from one of the caches, before attempting to access main memory (i.e. the disks), thereby decreasing the access time of requested memory by accessing the main memory less frequently as taught by La Fetra in col. 1, lines 25-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Dewey to further include Mathiske's bag-to-set buffering system. By doing so, Dewey would have a means of preventing data loss by mitigating the dangers of data buffer overflow in his RAM devices by writing the data to a backup memory (i.e. global) before such an overflow occurs, rather being restricted to preventing data loss only in the case of a controller failure as presently taught by Dewey in col. 11, line 66 through col. 12, line 12.

Response to Arguments

9. Applicant's amendments and arguments with respect to claims 5-7, 12, 13, and 17-19 have been fully considered, but are moot in view of the new ground(s) of rejection.

It is worthy to note that Applicant contends on page 12 of the Remarks section, "[t]he references to do not disclose a dedicated data transfer path over which one local cache transmits data to another local cache, which is recited as a transmitting step and a writing step".

Examiner maintains that Dewey does in fact teach a "dedicated data transfer path between at least two local cache memories of the channel control units". Referring to Fig. 7, Dewey discloses a dedicated path from the RAM (422), through the memory

interface (420), via the single dump link (426), back to the second memory interface (420'), which terminates at the second cache (422'). The path as described by Dewey is used to transfer data (read from or written to the RAM) between the channel control units.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
4-19-07